We claim:

1. A speech recognition device, comprising a similarity circuit that receives input signals composed of multi-dimensional vectors corresponding to the spectrum envelope of speech inputs to be recognized and puts out characteristics based on the self-organizing algorithm, and a matrix circuit that performs matrix operations of the output signals of said similarity circuit, wherein said similarity circuit comprises a circuit to calculate a distance between said multi-dimensional input vector and a pattern vector prepared in advance for speech recognition, calculates a value corresponding to one dimension using a pair of neuron MOSFETs for each dimension, and forms a voltage signal in accordance with the degree of similarity by summing the current that flows through each neuron MOSFET; and said matrix circuit, in which capacitors corresponding to weighing operations are arranged in matrix, receives the voltage signal in accordance with said degree of similarity and puts out what is most similar to said patterns prepared in advance from among the matrix operation results as the recognition result.

2. A speech recognition device, as set forth in claim 1, wherein said two neuron MOSFETs are of n-channel type and the drains of neuron MOSFETs for plural dimensions corresponding to the spectrum envelope of speech input are connected commonly to sum the drain current; said summed drain current is made to flow into a p-channel MOSFET that converts the drain current into a voltage signal; the connection node, to which the drain of said p-channel MOSFET and the drains of the neuron MOSFETs commonly connected are connected, is connected to one of inputs of an operational amplifier circuit; the output voltage of said operational amplifier circuit is supplied to the gate of said p-channel MOSFET; and the other input of said operational amplifier circuit is provided with an bias voltage that operates said neuron

MOSFET in a saturation area and said p-channel MOSFET, in a non-saturation area.

3. A speech recognition device, as set forth in claim 2, wherein said operational amplifier circuit has a common input and comprises a first and a second source follower output circuit having an identical circuit constant; the output signal of said first source follower output circuit is supplied to the gate of said p-channel MOSFET; and the output signal of said second source follower output circuit is supplied to said matrix circuit as an input voltage.

4. A speech recognition device, as set forth in claim 2, wherein dummy capacitances are added to said matrix circuit if necessary to equalize the input capacitance of plural input terminals to each other.

5. A speech recognition device, as set forth in claim 4, wherein said matrix circuit is provided with a comparison capacitor in accordance with an input signal; plural voltage comparison circuits, which regard the voltage formed by said comparison capacitor as a reference voltage and correspond to the speech recognition outputs that receive each matrix operation output, respectively, are provided; and a speech recognition output is obtained from each voltage comparison circuit.

6. A speech recognition device, as set forth in claim 1, wherein each of said circuit blocks is formed on a substrate that constitutes an integrated circuit.

7. A speech recognition device, as set forth in claim 2, wherein each of said circuit blocks is formed on a substrate that constitutes an integrated circuit.

8. A speech recognition device, as set forth in claim 3, wherein each of said circuit blocks is formed on a substrate that constitutes an integrated circuit.

9. A speech recognition device, as set forth in claim 4, wherein each of said circuit blocks is formed on a substrate that constitutes an integrated circuit.

10. A speech recognition device, as set forth in claim 5, wherein each of said circuit blocks is formed on a substrate that constitutes an integrated circuit.